WHAT IS CLAIMED IS:

1. A method of forming a semiconductor device comprising:

forming a gate pattern that includes a gate electrode on a substrate;

forming lightly doped impurity diffusion layers in the substrate at both sides of the gate pattern;

forming spacers on sidewalls of the gate pattern, the spacers having a bottom width;

implanting impurity ions using the gate pattern and the spacer as a mask to form a heavily doped impurity diffusion layer in the substrate;

removing the spacers; and

forming a conformal etch stop layer on the gate pattern and the substrate, wherein the etch stop layer is formed to a thickness of at least the bottom width of the spacers.

2. The method of Claim 1, further comprising:

forming a conformal etch shield layer on the gate pattern and the substrate, wherein the etch shield layer is formed of insulation material having etch selectivity with respect to the spacers; and

wherein the step of forming spacers comprises forming spacers on the etch shield layer on opposite sidewalls of the gate pattern.

3. The method of Claim 2, further forming a conformal buffer insulation layer the gate pattern and the substrate; and

wherein forming a conformal etch shield layer further comprises forming a conformal etch shield layer on the conformal buffer insulation layer.

4. The method of Claim 2, wherein the spacers comprise silicon oxide and the etch shield layer comprise silicon nitride.

5. The method of Claim 1, wherein the heavily doped impurity diffusion layer has a higher impurity concentration than the lightly doped impurity diffusion layer; and

wherein the lightly and heavily doped impurity diffusion layers are formed to

provide a lightly doped drain structure.

6. The method of Claim 1, wherein the etch stop layer is formed to a thickness substantially identical to the bottom width of the spacer.

7. The method of Claim 1, further comprising:

forming an interlayer insulation layer on the etch stop layer;

successively patterning the interlayer insulation layer and the etch stop layer to form a contact hole that exposes at least the heavily doped impurity diffusion layer; and

forming a conductive pattern that fills the contact hole.

8. The method of Claim 7, wherein the etch stop layer is formed of insulation material having etch selectivity with respect to the interlayer insulation layer.

9. The method of Claim 8, wherein the interlayer insulation layer comprises silicon oxide, and the etch stop layer comprises silicon nitride.

10. The method of Claim 7, wherein successively patterning the interlayer insulation layer and the etch stop layer, comprises:

patterning the interlayer insulation layer to expose at least the etch stop layer on the heavily doped impurity diffusion layer; and

anisotropically etching the exposed etch stop layer to form a contact hole that exposes at least the heavily doped impurity diffusion layer.

11. The method of Claim 10, wherein the contact hole further exposes a portion of the gate electrode in the gate pattern.

12. A method of forming a semiconductor device comprising:

forming a device isolation layer in a substrate to define first and second active regions;

forming a first gate pattern on the first active region and a second gate pattern on the second active region, wherein the first gate pattern comprises a first

gate insulation layer, a first gate electrode, and a first hard mask layer that are stacked, and the second gate pattern comprises a second gate insulation layer, a second gate electrode, and a second hard mask layer that are stacked;

forming a lightly doped impurity diffusion layer in the first active region at both sides of the first gate pattern;

forming spacers on sidewalls of the first and second gate patterns, the sidewall spacers having a bottom width;

forming a heavily doped impurity diffusion layer in the first active region using the first gate pattern and the spacers on the sidewalls of the first gate pattern as a mask;

removing the spacers; and

forming a conformal etch stop layer on the first and second gate patterns and the substrate,

wherein the second gate pattern is formed to cross over the device isolation layer and to reach the first active region, and

wherein the etch stop layer is formed to a thickness of at least the bottom width of the sidewall spacers.

13. The method of Claim 12, further comprising forming a conformal etch shield layer on the first and second gate patterns and the substrate, wherein the etch shield layer is formed of insulation material having etch selectivity with respect to the spacers; and

wherein forming spacers comprises forming spacers on the etch shield layer on opposite sidewalls of the first and second gate patterns.

14. The method of Claim 13, further comprising forming a conformal buffer insulation layer on the first and second gate patterns and the substrate; and

wherein forming a conformal etch shield layer comprises forming a conformal etch shield layer on the buffer insulation layer.

15. The method of Claim 13, wherein the spacers comprise silicon oxide, and the etch shield layer comprises silicon nitride.

16. The method of Claim 12, wherein the heavily doped impurity diffusion

layer has a higher impurity concentration than the lightly doped impurity diffusion layer, and wherein the lightly and heavily doped impurity diffusion layers are formed to provide a lightly doped drain structure.

17. The method of Claim 12, wherein the etch stop layer is formed to a thickness substantially identical to the bottom width of the spacers.

18. The method of Claim 12, further comprising:

forming an interlayer insulation layer on the etch stop layer;

successively patterning the interlayer insulation layer and the etch stop layer to form a contact hole that exposes the heavily doped impurity diffusion layer and a portion of the second gate electrode; and

forming a conductive pattern to fill the contact hole.

19. The method of Claim 18, wherein the etch stop layer comprises an insulation material having etch selectivity with respect to the interlayer insulation layer.

20. The method of Claim 19, wherein the interlayer insulation layer comprises silicon oxide, and the etch stop layer comprises silicon nitride

21. The method of Claim 18, wherein successively patterning the interlayer insulation layer and the etch stop layer comprises:

patterning the interlayer insulation layer to expose a portion of the etch stop layer that is located on the heavily and lightly doped impurity diffusion layers and a predetermined region of a top surface of the second gate pattern; and

successively etching the exposed etch stop layer and the second hard mask layer to form a contact hole that exposes the heavily doped impurity diffusion layer and a portion of the second gate electrode.